

Preliminary W28F321BT/TT



32MBIT (2MBIT × 16) PAGE MODE DUAL WORK FLASH MEMORY

1. GENERAL DESCRIPTION

The W28F321, a 4-Plane Page Mode Dual Work (Simultaneous Read while Erase/Program) Flash memory, is a low power, high density, cost efficiency, nonvolatile read/write storage solution for a wide range of applications. The product can be operated at $V_{DD} = 2.7V$ to $3.6V$ and $V_{PP} = 1.65V$ to $3.6V$ or $11.7V$ to $12.3V$. Its low voltage operation capability greatly extends battery life for portable applications.

The W28F321 provides high performance asynchronous page mode. It allows code execution directly from Flash, thus eliminating time-consuming wait states. Furthermore, its newly configurative partitioning architecture allows flexible dual work operation.

The memory array block architecture utilizes Enhanced Data Protection features, and provides separate Parameter and Main Blocks that provide maximum flexibility for safe nonvolatile code and data storage.

Fast program capability is provided through the use of high speed Page Buffer Program. Special OTP (One Time Program) block provides an area to store permanent code such as a unique number.

2. FEATURES

- 32M Density with 16 Bit I/O Interface
 - $5 \mu S$ / Word (Typ.) at $12V V_{PP}$
- High-Performance Reads
 - 70/25 nS 8-Word Page Mode
- Configurative 4-Plane Dual Work
 - Flexible Partitioning
 - Read operations during Block Erase or (Page Buffer) Program
 - Status Register for Each Partition
- Low Power Operation
 - 2.7V Read and Write Operations
 - Automatic Power Savings Mode Reduces
- Enhanced Code + Data Storage
 - $5 \mu S$ Typical Erase/Program Suspends
- OTP (One Time Program) Block
 - 4-Word Factory-Programmed Area
 - 4-Word User-Programmed Area
- High Performance Program with Page Buffer
 - 16-Word Page Buffer
- Operating Temperature
 - $-40^{\circ}C$ to $+85^{\circ}C$
- CMOS Process (P-type silicon substrate)
- Flexible Blocking Architecture
 - Eight 4k-word Parameter Blocks
 - Sixty-three 32k-word Main Blocks
 - Top or Bottom Parameter Location
- Enhanced Data Protection Features
 - Individual Block Lock and Block Lock-Down with Zero-Latency
 - All blocks are locked at power-up or device reset
 - Absolute Protection with $V_{PP} \leq V_{PPLK}$
 - Block Erase, Full Chip Erase, (Page Buffer) Word Program Lockout during Power Transitions
- Automated Erase/Program Algorithms

- 3.0V Low-Power 11 μ S/ Word (Typ.) Programming
 - 12V No Glue Logic 9 μ S/ Word (Typ.) Production Programming and 0.5s Erase (Typ.)
 - Cross-Compatible Command Support
 - Common Flash Interface (CFI)
 - Basic Command Set
 - Extended Cycling Capability
 - Minimum 100,000 Block Erase Cycles
 - Chip-Size Packaging
 - 48-Pin (12 mm x 20 mm) TSOP
 - ETOX™ Flash Technology
 - No designed or rated as radiation hardened
- * ETOX is a trademark of Intel Corporation.*

3. PIN CONFIGURATION

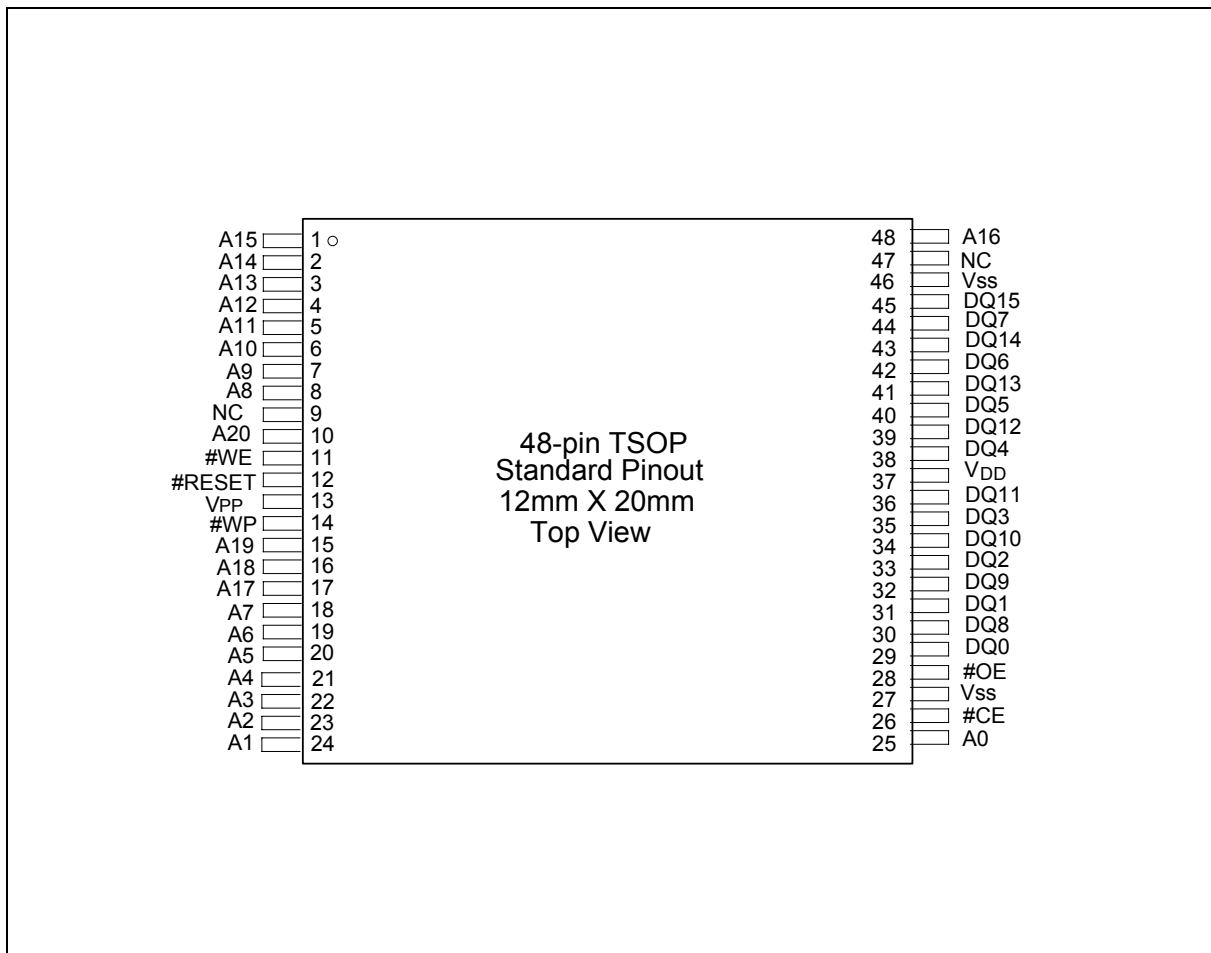


Figure 1. 48-Lead TSOP (Normal Bend) Pinout

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Table 1. Pin Descriptions

SYMBOL	TYPE	NAME AND FUNCTION
A0 – A20	INPUT	ADDRESS INPUTS: Inputs for addresses. 32M: A0 – A20.
DQ0 – DQ15	INPUT/ OUTPUT	DATA INPUT/OUTPUTS: Inputs data and commands during CUI (Command User Interface) write cycles, outputs data during memory array, status register, query code, identifier code and partition configuration register code reads. Data pins float to high impedance (High Z) when the chip or outputs are deselected. Data is internally latched during an erase or program cycle.
#CE	INPUT	CHIP ENABLE: Activates the device's control logic, input buffers, decoders and sense amplifiers. #CE-high (V_{IH}) deselected the device and reduces power consumption to standby levels.
#RESET	INPUT	RESET: When low (V_{IL}), #RESET resets internal automation and inhibits write operations, which provides data protection. #RESET-high (V_{IH}) enables normal operation. After power-up or reset mode, the device is automatically set to read array mode. #RESET must be low during power-up/down.
#OE	INPUT	OUTPUT ENABLE: Gates the device's outputs during a read cycle.
#WE	INPUT	WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of #CE or #WE (whichever goes high first).
#WP	INPUT	WRITE PROTECT: When #WP is V_{IL} , locked-down blocks cannot be unlocked. Erase or program operation can be executed to the blocks which are not locked and locked-down. When #WP is V_{IH} , lock-down is disabled.
V_{PP}	INPUT	MONITORING POWER SUPPLY VOLTAGE: V_{PP} is not used for power supply pin. With $V_{PP} \leq V_{PPLK}$, block erase, full chip erase, (page buffer) program or OTP program cannot be executed and should not be attempted. Applying $12V \pm 0.3V$ to V_{PP} provides fast erasing or fast programming mode. In this mode, V_{PP} is power supply pin. Applying $12V \pm 0.3V$ to V_{PP} during erase/program can only be done for a maximum of 1,000 cycles on each block. V_{PP} may be connected to $12V \pm 0.3V$ for a total of 80 hours maximum. Use of this pin at 12V beyond these limits may reduce block cycling capability or cause permanent damage.
V_{DD}	SUPPLY	DEVICE POWER SUPPLY (2.7V to 3.6V): With $V_{DD} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{DD} voltage (see DC Characteristics) produce spurious results and should not be attempted.
V_{SS}	SUPPLY	GROUND: Do not float any ground pins.
NC		NO CONNECT: Lead is not internally connected; it may be driven or floated.

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Table 2. Simultaneous Operation Modes Allowed with Four Planes^(1,2)

IF ONE PARTITION IS:	THEN THE MODES ALLOWED IN THE OTHER PARTITION IS:										
	Read Array	Read ID/OTP	Read Status	Read Query	Word Program	Page Buffer Program	OTP Program	Block Erase	Full Chip Erase	Program Suspend	Block Erase Suspend
Read Array	X	X	X	X	X	X		X		X	X
Read ID/OTP	X	X	X	X	X	X		X		X	X
Read Status	X	X	X	X	X	X	X	X	X	X	X
Read Query	X	X	X	X	X	X		X		X	X
Word Program	X	X	X	X							X
Page Buffer Program	X	X	X	X							X
OTP Program			X								
Block Erase	X	X	X	X							
Full Chip Erase			X								
Program Suspend	X	X	X	X							X
Block Erase Suspend	X	X	X	X	X	X				X	

Notes:

- "X" denotes the operation available.
- Configurative Partition Dual Work Restrictions:
 Status register reflects partition state, not WSM (Write State Machine) state - this allows a status register for each partition.
 Only one partition can be erased or programmed at a time - no command queuing.
 Commands must be written to an address within the block targeted by that command.

BLOCK NUMBER		ADDRESS RANGE	BLOCK NUMBER		ADDRESS RANGE		
PLANE3 (PARAMETER PLANE)	70	4K-WORD	1FF000h - 1FFFFFFh	PLANE1 (UNIFORM PLANE)	31	32K-WORD	0F8000h - 0FFFFFFh
	69	4K-WORD	1FE000h - 1FEFFFFh		30	32K-WORD	0F0000h - 0F7FFFFh
	68	4K-WORD	1FD000h - 1FDFFFFh		29	32K-WORD	0E8000h - 0EFFFFFFh
	67	4K-WORD	1FC000h - 1FCFFFFh		28	32K-WORD	0E0000h - 0E7FFFFh
	66	4K-WORD	1FB000h - 1FBFFFFh		27	32K-WORD	0D8000h - 0DFFFFFFh
	65	4K-WORD	1FA000h - 1FAFFFFh		26	32K-WORD	0D0000h - 0D7FFFFh
	64	4K-WORD	1F9000h - 1F9FFFFh		25	32K-WORD	0C8000h - 0CFFFFFFh
	63	4K-WORD	1F8000h - 1F8FFFFh		24	32K-WORD	0C0000h - 0C7FFFFh
	62	32K-WORD	1F0000h - 1F7FFFFh		23	32K-WORD	0B8000h - 0BFFFFFFh
	61	32K-WORD	1E8000h - 1EFFFFFFh		22	32K-WORD	0B0000h - 0B7FFFFh
	60	32K-WORD	1E0000h - 1E7FFFFh		21	32K-WORD	0A8000h - 0AFFFFFFh
	59	32K-WORD	1D8000h - 1DFFFFFFh		20	32K-WORD	0A0000h - 0A7FFFFh
	58	32K-WORD	1D0000h - 1D7FFFFh		19	32K-WORD	098000h - 09FFFFFFh
	57	32K-WORD	1C8000h - 1CFFFFFFh		18	32K-WORD	090000h - 097FFFFh
	56	32K-WORD	1C0000h - 1C7FFFFh		17	32K-WORD	088000h - 08FFFFFFh
	55	32K-WORD	1B8000h - 1BFFFFFFh		16	32K-WORD	080000h - 087FFFFh
	54	32K-WORD	1B0000h - 1B7FFFFh	PLANE0 (UNIFORM PLANE)	15	32K-WORD	078000h - 07FFFFFFh
	53	32K-WORD	1A8000h - 1AFFFFFFh		14	32K-WORD	070000h - 077FFFFh
	52	32K-WORD	1A0000h - 1A7FFFFh		13	32K-WORD	068000h - 06FFFFFFh
	51	32K-WORD	198000h - 19FFFFFFh		12	32K-WORD	060000h - 067FFFFh
50	32K-WORD	190000h - 197FFFFh	11		32K-WORD	058000h - 05FFFFFFh	
49	32K-WORD	188000h - 18FFFFFFh	10		32K-WORD	050000h - 057FFFFh	
48	32K-WORD	180000h - 187FFFFh	9		32K-WORD	048000h - 04FFFFFFh	
PLANE2 (UNIFORM PLANE)	47	32K-WORD	178000h - 17FFFFFFh		8	32K-WORD	040000h - 047FFFFh
	46	32K-WORD	170000h - 177FFFFh		7	32K-WORD	038000h - 03FFFFFFh
	45	32K-WORD	168000h - 16FFFFFFh		6	32K-WORD	030000h - 037FFFFh
	44	32K-WORD	160000h - 167FFFFh	5	32K-WORD	028000h - 02FFFFFFh	
	43	32K-WORD	158000h - 15FFFFFFh	4	32K-WORD	020000h - 027FFFFh	
	42	32K-WORD	150000h - 157FFFFh	3	32K-WORD	018000h - 01FFFFFFh	
	41	32K-WORD	148000h - 14FFFFFFh	2	32K-WORD	010000h - 017FFFFh	
	40	32K-WORD	140000h - 147FFFFh	1	32K-WORD	008000h - 00FFFFFFh	
	39	32K-WORD	138000h - 13FFFFFFh	0	32K-WORD	000000h - 007FFFFh	
	38	32K-WORD	130000h - 137FFFFh				
	37	32K-WORD	128000h - 12FFFFFFh				
	36	32K-WORD	120000h - 127FFFFh				
	35	32K-WORD	118000h - 11FFFFFFh				
	34	32K-WORD	110000h - 117FFFFh				
	33	32K-WORD	108000h - 10FFFFFFh				
	32	32K-WORD	100000h - 107FFFFh				

Figure 2.1 Top Parameter Memory Map

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BLOCK NUMBER		ADDRESS RANGE	BLOCK NUMBER		ADDRESS RANGE		
PLANE3 (UNIFORM PLANE)	70	32K-WORD	1F8000H - 1FFFFFFH	PLANE1 (UNIFORM PLANE)	38	32K-WORD	0F8000H - 0FFFFFFH
	69	32K-WORD	1F0000H - 1F7FFFH		37	32K-WORD	0F0000H - 0F7FFFH
	68	32K-WORD	1E8000H - 1EFFFFH		36	32K-WORD	0E8000H - 0EFFFFH
	67	32K-WORD	1E0000H - 1E7FFFH		35	32K-WORD	0E0000H - 0E7FFFH
	66	32K-WORD	1D8000H - 1DFFFFH		34	32K-WORD	0D8000H - 0DFFFFH
	65	32K-WORD	1D0000H - 1D7FFFH		33	32K-WORD	0D0000H - 0D7FFFH
	64	32K-WORD	1C8000H - 1CFFFFH		32	32K-WORD	0C8000H - 0CFFFFH
	63	32K-WORD	1C0000H - 1C7FFFH		31	32K-WORD	0C0000H - 0C7FFFH
	62	32K-WORD	1B8000H - 1BFFFFH		30	32K-WORD	0B8000H - 0BFFFFH
	61	32K-WORD	1B0000H - 1B7FFFH		29	32K-WORD	0B0000H - 0B7FFFH
	60	32K-WORD	1A8000H - 1AFFFFH		28	32K-WORD	0A8000H - 0AFFFFH
	59	32K-WORD	1A0000H - 1A7FFFH		27	32K-WORD	0A0000H - 0A7FFFH
	58	32K-WORD	198000H - 19FFFFH		26	32K-WORD	098000H - 09FFFFH
	57	32K-WORD	190000H - 197FFFH		25	32K-WORD	090000H - 097FFFH
56	32K-WORD	188000H - 18FFFFH	24	32K-WORD	088000H - 08FFFFH		
55	32K-WORD	180000H - 187FFFH	23	32K-WORD	080000H - 087FFFH		
PLANE2 (UNIFORM PLANE)	54	32K-WORD	178000H - 17FFFFH	PLANE0 (PARAMETER PLANE)	22	32K-WORD	078000H - 07FFFFH
	53	32K-WORD	170000H - 177FFFH		21	32K-WORD	070000H - 077FFFH
	52	32K-WORD	168000H - 16FFFFH		20	32K-WORD	068000H - 06FFFFH
	51	32K-WORD	160000H - 167FFFH		19	32K-WORD	060000H - 067FFFH
	50	32K-WORD	158000H - 15FFFFH		18	32K-WORD	058000H - 05FFFFH
	49	32K-WORD	150000H - 157FFFH		17	32K-WORD	050000H - 057FFFH
	48	32K-WORD	148000H - 14FFFFH		16	32K-WORD	048000H - 04FFFFH
	47	32K-WORD	140000H - 147FFFH		15	32K-WORD	040000H - 047FFFH
	46	32K-WORD	138000H - 13FFFFH		14	32K-WORD	038000H - 03FFFFH
	45	32K-WORD	130000H - 137FFFH		13	32K-WORD	030000H - 037FFFH
	44	32K-WORD	128000H - 12FFFFH		12	32K-WORD	028000H - 02FFFFH
	43	32K-WORD	120000H - 127FFFH		11	32K-WORD	020000H - 027FFFH
	42	32K-WORD	118000H - 11FFFFH		10	32K-WORD	018000H - 01FFFFH
	41	32K-WORD	110000H - 117FFFH		9	32K-WORD	010000H - 017FFFH
40	32K-WORD	108000H - 10FFFFH	8	32K-WORD	008000H - 00FFFFH		
39	32K-WORD	100000H - 107FFFH	7	4K-WORD	007000H - 007FFFH		
			6	4K-WORD	006000H - 006FFFH		
			5	4K-WORD	005000H - 005FFFH		
			4	4K-WORD	004000H - 004FFFH		
			3	4K-WORD	003000H - 003FFFH		
			2	4K-WORD	002000H - 002FFFH		
			1	4K-WORD	001000H - 001FFFH		
			0	4K-WORD	000000H - 000FFFH		

Figure 2.2 Bottom Parameter Memory Map

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Table 3. Identifier Codes and OTP Address for Read Operation

	CODE	ADDRESS [A15 – A0]	DATA [DQ15 – DQ0]	NOTES
Manufacture Code	Manufacture Code	0000H	00B0H	1
Device Code	Top Parameter	0001H	00B4H	1, 2
	Bottom Parameter		00B5H	1, 2
Block Lock Configuration Code	Block is Unlocked	Block Address +2	DQ0 = 0	3
	Block is Locked		DQ0 = 1	3
	Block is not Locked-Down		DQ1 = 0	3
	Block is Locked-Down		DQ1 = 1	3
Device Configuration Code	Partition Configuration register	0006H	PCRC	1, 4
OTP	OTP Lock	0080H	OTP-LK	1, 5
	OTP	0081-0088H	OTP	1, 6

Notes:

1. The address A20 – A16 are shown in below table for reading the manufacturer, device, lock configuration, device configuration code and OTP data.
2. Top parameter device has its parameter blocks in the plane3 (The highest address).
Bottom parameter device has its parameter blocks in the plane0 (The lowest address).
3. Block Address = The beginning location of a block address within the partition to which the Read Identifier Codes/OTP command (90H) has been written.
DQ15 – DQ2 are reserved for future implementation.
4. PCRC = Partition Configuration Register Code.
5. OTP-LK = OTP Block Lock configuration.
6. OTP = OTP Block data.

Table 4. Identifier Codes and OTP Address for Read Operation on Partition Configuration⁽¹⁾

PARTITION CONFIGURATION REGISTER ⁽²⁾			ADDRESS (32M-bit device) [A20 – A16]
PCR.10	PCR.9	PCR.8	
0	0	0	00H
0	0	1	00H or 08H
0	1	0	00H or 10H
1	0	0	00H or 18H
0	1	1	00H or 08H or 10H
1	1	0	00H or 10H or 18H
1	0	1	00H or 08H or 18H
1	1	1	00H or 08H or 10H or 18H

Notes:

1. The address to read the identifier codes or OTP data is dependent on the partition which is selected when writing the Read Identifier Codes/OTP command (90H).
2. Refer to Table 12 for the partition configuration register.

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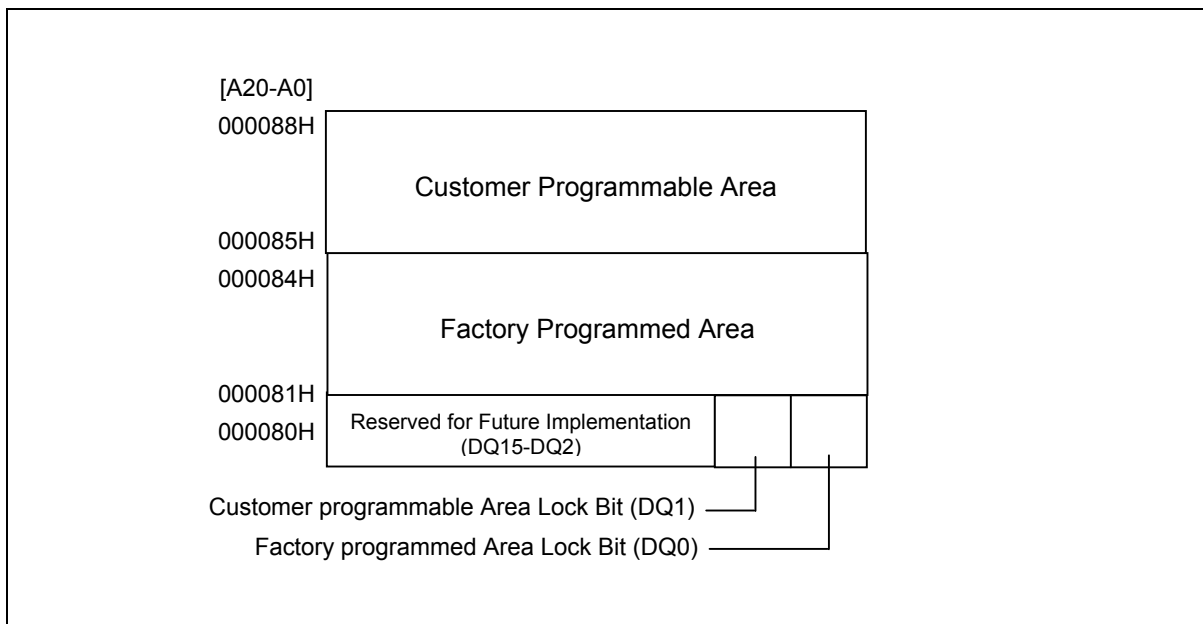


Figure 3. OTP Block Address Map for OTP Program (The area outside 80H~88H cannot be used.)

Table 5. Bus Operations (1, 2)

MODE	NOTE	#RESET	#CE	#OE	#WE	ADDRESS	V _{PP}	DQ0 – 15
Read Array	6	V _{IH}	V _{IL}	V _{IL}	V _{IH}	X	X	DOUT
Output Disable		V _{IH}	V _{IL}	V _{IH}	V _{IH}	X	X	High Z
Standby		V _{IH}	V _{IH}	X	X	X	X	High Z
Reset	3	V _{IL}	X	X	X	X	X	High Z
Read Identifier Codes/OTP	6	V _{IH}	V _{IL}	V _{IL}	V _{IH}	See Table 3, 4	X	See Table 3, 4
Read Query	6,7	V _{IH}	V _{IL}	V _{IL}	V _{IH}	See Appendix	X	See Appendix
Write	4,5,6	V _{IH}	V _{IL}	V _{IH}	V _{IL}	X	X	DIN

Notes:

1. Refer to DC Characteristics. When $V_{PP} \leq V_{PPLK}$, memory contents can be read, but cannot be altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or V_{PPH1/2} for V_{PP}. See DC Characteristics for V_{PPLK} and V_{PPH1/2} voltages.
3. #RESET at V_{SS} ±0.2V ensures the lowest power consumption.
4. Command writes involving block erase, full chip erase, (page buffer) program or OTP program are reliably executed when V_{PP} = V_{PPH1/2} and V_{DD} = 2.7V to 3.6V.
5. Refer to Table 6 for valid DIN during a write operation.
6. Never hold #OE low and #WE low at the same timing.
7. Refer to Appendix for more information about query code.

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Table 6. Command Definitions⁽¹¹⁾

COMMAND	BUS CYCLES REQ'D.	NOTE	FIRST BUS CYCLE			SECOND BUS CYCLE		
			Oper ⁽¹⁾	Addr ⁽²⁾	Data	Oper ⁽¹⁾	Addr ⁽²⁾	Data ⁽³⁾
Read Array	1		Write	PA	FFH			
Read Identifier Codes/OTP	≥2	4	Write	PA	90H	Read	IA or OA	ID or OD
Read Query	≥2	4	Write	PA	98H	Read	QA	QD
Read Status Register	2		Write	PA	70H	Read	PA	SRD
Clear Status Register	1		Write	PA	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Full Chip Erase	2	5,9	Write	X	30H	Write	X	D0H
Program	2	5,6	Write	WA	40H or 10H	Write	WA	WD
Page Buffer Program	≥4	5,7	Write	WA	E8H	Write	WA	N-1
Block Erase and (Page Buffer) Program Suspend	1	8,9	Write	PA	B0H			
Block Erase and (Page Buffer) Program Resume	1	8,9	Write	PA	D0H			
Set Block Lock Bit	2		Write	BA	60H	Write	BA	01H
Clear Block Lock Bit	2	10	Write	BA	60H	Write	BA	D0H
Set Block Lock-down Bit	2		Write	BA	60H	Write	BA	2FH
OTP Program	2	9	Write	OA	C0H	Write	OA	OD
Set Partition configuration Register	2		Write	PCRC	60H	Write	PCRC	04H

Notes:

- Bus operations are defined in Table 5.
- All addresses which are written at the first bus cycle should be the same as the addresses which are written at the second bus cycle.
 X = Any valid address within the device.
 PA = Address within the selected partition.
 IA = Identifier codes address (See Table 3 and Table 4).
 QA = Query codes address. Refer to Appendix for details.
 BA = Address within the block being erased, set/cleared block lock bit or set block lock-down bit.
 WA = Address of memory location for the Program command or the first address for the Page Buffer Program command.
 OA = Address of OTP block to be read or programmed (See Figure 3).
 PCRC = Partition configuration register code presented on the address A0 – A15.
- ID = Data read from identifier codes. (See Table 3 and Table 4).
 QD = Data read from query database. Refer to Appendix for details.
 SRD = Data read from status register. See Table 10 and Table 11 for a description of the status register bits.
 WD = Data to be programmed at location WA. Data is latched on the rising edge of #WE or #CE (whichever goes high first).
 OD = Data to be programmed at location OA. Data is latched on the rising edge of #WE or #CE (whichever goes high first).
 N-1 = N is the number of the words to be loaded into a page buffer.
- Following the Read Identifier Codes/OTP command, read operations access manufacturer code, device code, block lock configuration code, partition configuration register code and the data within OTP block (See Table 3 and Table 4). The Read Query command is available for reading CFI (Common Flash Interface) information.
- Block erase, full chip erase or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when #RESET is V_{IH}.
- Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.
- Following the third bus cycle, inputs the program sequential address and write data of "N" times. Finally, input the any valid address within the target partition to be programmed and the confirm command (D0H). Refer to Appendix for details.

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8. If the program operation in one partition is suspended and the erase operation in other partition is also suspended, the suspended program operation should be resumed first, and then the suspended erase operation should be resumed next.
9. Full chip erase and OTP program operations can not be suspended. The OTP Program command can not be accepted while the block erase operation is being suspended.
10. Following the Clear Block Lock Bit command, block which is not locked-down is unlocked when #WP is V_{IL} . When #WP is V_{IH} , lock-down bit is disabled and the selected block is unlocked regardless of lock-down configuration.
11. Commands other than those shown above are reserved by Winbond for future device implementations and should not be used.

Table 7. Functions of Block Lock⁽⁵⁾ and Block Lock-Down

CURRENT STATE					
State	#WP	DQ1 ⁽¹⁾	DQ0 ⁽¹⁾	State Name	Erase/Program Allowed ⁽²⁾
[000]	0	0	0	Unlocked	Yes
[001] ⁽³⁾	0	0	1	Locked	No
[011]	0	1	1	Locked-down	No
[100]	1	0	0	Unlocked	Yes
[101] ⁽³⁾	1	0	1	Locked	No
[110] ⁽⁴⁾	1	1	0	Lock-down Disable	Yes
[111]	1	1	1	Lock-down Disable	No

Notes:

1. DQ0 = 1: a block is locked; DQ0=0: a block is unlocked.
DQ1 = 1: a block is locked-down; DQ1=0: a block is not locked-down.
2. Erase and program are general terms, respectively, to express: block erase, full chip erase and (page buffer) program operations.
3. At power-up or device reset, all blocks default to locked state and are not locked-down, that is, [001] (#WP = 0) or [101] (#WP = 1), regardless of the states before power-off or reset operation.
4. When #WP is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.
5. OTP (One Time Program) block has the lock function, which is different from those described above.

Table 8. Block Locking State Transitions upon Command Write⁽⁴⁾

CURRENT STATE				RESULT AFTER LOCK COMMAND WRITTEN (Next State)		
State	#WP	DQ1	DQ0	Set Lock ⁽¹⁾	Clear Lock ⁽¹⁾	Set Lock-down ⁽¹⁾
[000]	0	0	0	[001]	No Change	[011] ⁽²⁾
[001]	0	0	1	No Change ⁽³⁾	[000]	[011]
[011]	0	1	1	No Change	No Change	No Change
[100]	1	0	0	[101]	No Change	[111] ⁽²⁾
[101]	1	0	1	No Change	[100]	[111]
[110]	1	1	0	[111]	No Change	[111] ⁽²⁾
[111]	1	1	1	No Change	[110]	No Change

Notes:

1. "Set Lock" means Set Block Lock Bit command, "Clear Lock" means Clear Block Lock Bit command and "Set Lock-down" means Set Block Lock-Down Bit command.

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2. When the Set Block Lock-Down Bit command is written to the unlocked block (DQ0 = 0), the corresponding block is locked-down and automatically locked at the same time.
3. "No Change" means that the state remains unchanged after the command written.
4. In this state transitions table, assumes that #WP is not changed and fixed V_{IL} or V_{IH}.

Table 9. Block Locking State Transitions upon #WP Transition⁽⁴⁾

PREVIOUS STATE	CURRENT STATE				RESULT AFTER #WP TRANSITION (Next State)	
	State	#WP	DQ1	DQ0	#WP = 0→1 ⁽¹⁾	#WP = 1→0 ⁽¹⁾
-	[000]	0	0	0	[100]	-
-	[001]	0	0	1	[101]	-
[110] ⁽²⁾	[011]	0	1	1	[110]	-
Other than [110] ⁽²⁾					[111]	-
-	[100]	1	0	0	-	[000]
-	[101]	1	0	1	-	[001]
-	[110]	1	1	0	-	[011] ⁽³⁾
-	[111]	1	1	1	-	[011]

Notes:

1. "#WP = 0→1" means that #WP is driven to V_{IH} and "#WP = 1→0" means that #WP is driven to V_{IL}.
2. State transition from the current state [011] to the next state depends on the previous state.
3. When #WP is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.
4. In this state transitions table, assumes that lock configuration commands are not written in previous, current and next state.

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Table 10. Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
WSMS	BESS	BEFCES	PBPOPS	VPPS	PBPSS	DPS	R
7	6	5	4	3	2	1	0
<p>SR.15 – SR.8 = RESERVED FOR FUTURE ENHANCEMENTS (R)</p> <p>SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy</p> <p>SR.6 = BLOCK ERASE SUSPEND STATUS (BESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed</p> <p>SR.5 = BLOCK ERASE AND FULL CHIP ERASE STATUS (BEFCES) 1 = Error in Block Erase or Full Chip Erase 0 = Successful Block Erase or Full Chip Erase</p> <p>SR.4 = (PAGE BUFFER) PROGRAM AND OTP PROGRAM STATUS (PBPOPS) 1 = Error in (Page Buffer) Program or OTP Program 0 = Successful (Page Buffer) Program or OTP Program</p> <p>SR.3 = V_{PP} STATUS (VPPS) 1 = V_{PP} LOW Detect, Operation Abort 0 = V_{PP} OK</p> <p>SR.2 = (PAGE BUFFER) PROGRAM SUSPEND STATUS (PBPSS) 1 = (Page Buffer) Program Suspended 0 = (Page Buffer) Program in Progress/Completed</p> <p>SR.1 = DEVICE PROTECT STATUS (DPS) 1 = Erase or Program Attempted on a Locked Block, Operation Abort 0 = Unlocked</p> <p>SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)</p>				<p>NOTES:</p> <p>Status Register indicates the status of the partition, not WSM (Write State Machine). Even if the SR.7 is "1", the WSM may be occupied by the other partition when the device is set to 2, 3 or 4 partitions configuration.</p> <p>Check SR.7 to determine block erase, full chip erase, (page buffer) program or OTP program completion. SR.6 – SR.1 are invalid while SR.7 = "0".</p> <p>If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, (page buffer) program, set/clear block lock bit, set block lock-down bit, set partition configuration register attempt, an improper command sequence was entered.</p> <p>SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. SR.3 is not guaranteed to report accurate feedback when V_{PP} ≠ V_{PPH1}, V_{PPH2} or V_{PPLK}.</p> <p>SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes/OTP command indicates block lock bit status.</p> <p>SR.15 – SR.8 and SR.0 are reserved for future use and should be masked out when polling the status register.</p>			

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Table 11. Extended Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

<p>XSR.15 – 8 = RESERVED FOR FUTURE ENHANCEMENTS (R)</p> <p>XSR.7 = STATE MACHINE STATUS (SMS) 1 = Page Buffer Program available 0 = Page Buffer Program not available</p> <p>XSR.6 – 0 = RESERVED FOR FUTURE ENHANCEMENTS (R)</p>	<p style="text-align: center;">NOTES:</p> <p>After issue a Page Buffer Program command (E8H), XSR.7 = "1" indicates that the entered command is accepted. XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not.</p> <p>XSR.15 – 8 and XSR.6 – 0 are reserved for future use and should be masked out when polling the extended status register.</p>
--	--



Table 12. Partition Configuration Register Definition

R	R	R	R	R	PC2	PC1	PC0
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

<p>PCR.15 – 11 = RESERVED FOR FUTURE ENHANCEMENTS (R)</p> <p>PCR.10 – 8 = PARTITION CONFIGURATION (PC2 – 0)</p> <p>000 = No partitioning. Dual Work is not allowed.</p> <p>001 = Plane1 – 3 are merged into one partition. (default in a bottom parameter device)</p> <p>010 = Plane 0 – 1 and Plane2 – 3 are merged into one partition respectively.</p> <p>100 = Plane 0 – 2 are merged into one partition. (default in a top parameter device)</p> <p>011 = Plane 2 – 3 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.</p> <p>110 = Plane 0 – 1 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.</p> <p>101 = Plane 1 – 2 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.</p>	<p>111 = There are four partitions in this configuration. Each plane corresponds to each partition respectively. Dual work operation is available between any two partitions.</p> <p>PCR.7 – 0 = RESERVED FOR FUTURE ENHANCEMENTS (R)</p> <p>NOTES:</p> <p>After power-up or device reset, PCR10-8 (PC2 – 0) is set to "001" in a bottom parameter device and "100" in a top parameter device.</p> <p>See Figure 4 for the detail on partition configuration.</p> <p>PCR.15 – 11 and PCR.7 – 0 are reserved for future use and should be masked out when polling the partition configuration register.</p>
--	--

PC2 PC1 PC0	PARTITIONING FOR DUAL WORK	PC2 PC1 PC0	PARTITIONING FOR DUAL WORK
0 0 0	<p style="text-align: center;">PARTITION0</p>	0 1 1	<p style="text-align: center;">PARTITION2 PARTITION1 PARTITION0</p>
0 0 1	<p style="text-align: center;">PARTITION1 PARTITION0</p>	1 1 0	<p style="text-align: center;">PARTITION2 PARTITION1 PARTITION0</p>
0 1 0	<p style="text-align: center;">PARTITION1 PARTITION0</p>	1 0 1	<p style="text-align: center;">PARTITION2 PARTITION1 PARTITION0</p>
1 0 0	<p style="text-align: center;">PARTITION1 PARTITION0</p>	1 1 1	<p style="text-align: center;">PARTITION3 PARTITION2 PARTITION1 PARTITION0</p>

Figure 4. Partition Configuration

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4. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings*

Operating Temperature	
During Read, Erase and Program	-40°C to +85°C ⁽¹⁾
Storage Temperature	
During under Bias	-40°C to +85°C
During non Bias	-65°C to +125°C
Voltage On Any Pin	
(except V _{DD} and V _{PP})	-0.5V to V _{DD} +0.5V ⁽²⁾
V _{DD} Supply Voltage.....	-0.2V to +3.9V ⁽²⁾
V _{PP} Supply Voltage.....	-0.2V to +12.6V ^(2,3,4)
Output Short Circuit Current.....	100 mA ⁽⁵⁾

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Notes:

1. Operating temperature is for extended temperature product defined by this specification.
2. All specified voltages are with respect to V_{SS}. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{DD} and V_{PP} pins. During transitions, this level may undershoot to -2.0V for periods <20 nS. Maximum DC voltage on input/output pins and V_{DD} is V_{DD} +0.5V, which, during transitions, may overshoot to V_{DD} +2.0V for periods <20 nS.
3. Maximum DC voltage on V_{PP} may overshoot to +13.0V for periods <20 nS.
4. V_{PP} erase/program voltage is normally 2.7V to 3.6V. Applying 11.7V to 12.3V to V_{PP} during erase/program can be done for a maximum of 1,000 cycles on the main blocks and 1,000 cycles on the parameter blocks. V_{PP} may be connected to 11.7V to 12.3V for a total of 80 hours maximum.
5. Output shorted for no more than one second. No more than one output shorted at a time.

Operating Conditions

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	NOTE
Operating Temperature	TA	-40	+25	+85	°C	
V _{DD} Supply Voltage	V _{DD}	2.7	3.0	3.6	V	1
V _{PP} Voltage when Used as a Logic Control	V _{PPH1}	1.65	3.0	3.6	V	1
V _{PP} Supply Voltage	V _{PPH2}	11.7	12	12.3	V	1, 2
Main Block Erase Cycling: V _{PP} = 3.0V		100,000			Cycles	
Parameter Block Erase Cycling: V _{PP} = 3.0V		100,000			Cycles	
Main Block Erase Cycling: V _{PP} = 12V, 80 hrs.				1,000	Cycles	
Parameter Block Erase Cycling: V _{PP} = 12V, 80 hrs.				1,000	Cycles	
Maximum V _{PP} hours at 12V				80	Hours	

Notes:

1. See DC Characteristics tables for voltage range-specific specification.
2. Applying V_{PP} = 11.7V to 12.3V during an erase or program can be done for a maximum of 1,000 cycles on the main blocks and 1,000 cycles on the parameter blocks. A permanent connection to V_{PP} = 11.7V to 12.3V is not allowed and can cause damage to the device.

Capacitance⁽¹⁾

T_A = +25° C, f = 1 MHz

PARAMETER	SYM.	TYP.	MAX.	UNIT	CONDITION
Input Capacitance	C _{IN}	4	7	pF	V _{IN} = 0.0V
Output Capacitance	C _{OUT}	6	10	pF	V _{OUT} = 0.0V

Note: Sampled, not 100% tested.

AC Input/Output Test Conditions

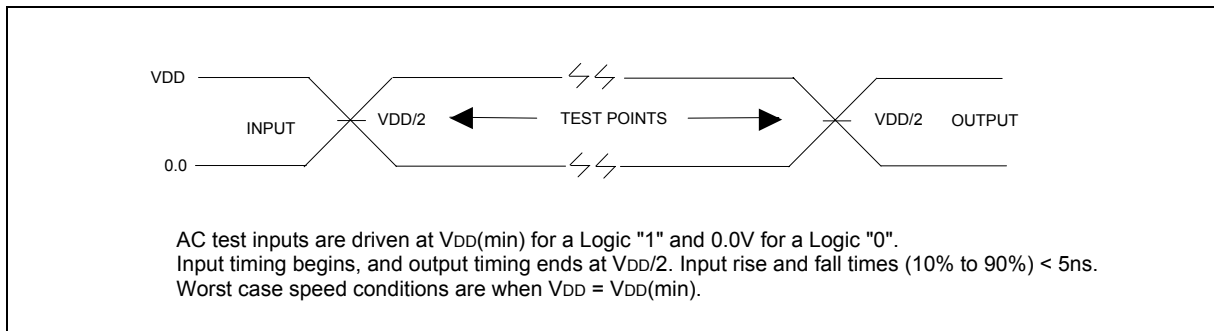


Figure 5. Transient Input/Output Reference Waveform for V_{DD} = 2.7V to 3.6V

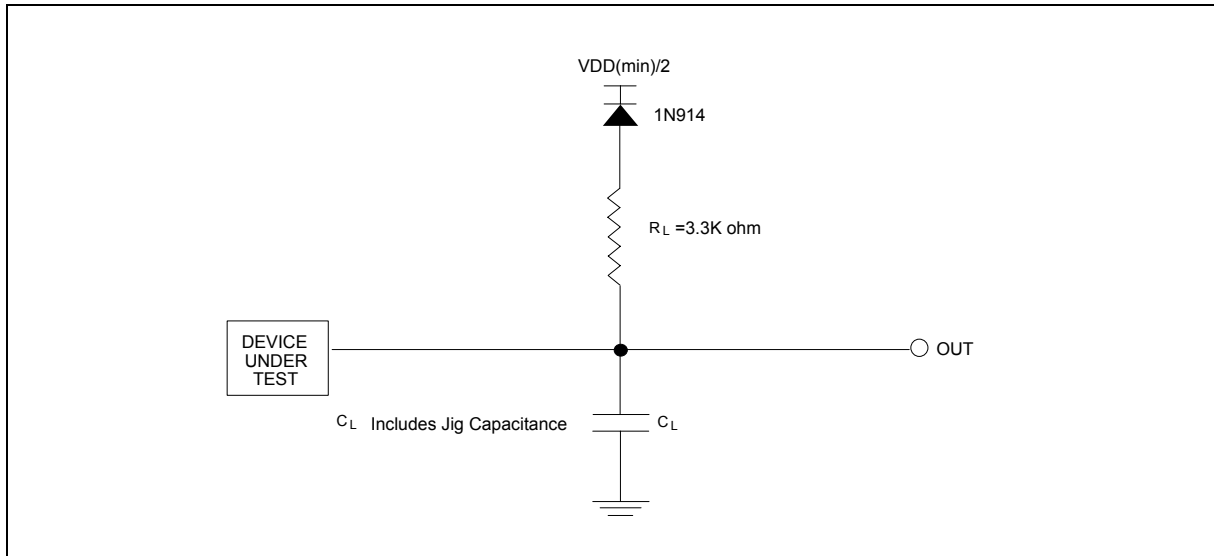


Figure 6. Transient Equivalent Testing Load Circuit

Table 13. Configuration Capacitance Loading Value

TEST CONFIGURATION	C _L (PF)
V _{DD} = 2.7V to 3.6V	50

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DC Characteristics

PARAMETER	SYM.	TEST CONDITIONS	V _{DD} = 2.7V to 3.6V			UNIT
			Min.	Typ.	Max.	
Input Load Current (note 1)	I _{LI}	V _{DD} = V _{DD} Max., V _{IN} /V _{OUT} = V _{DD} or V _{SS}	-1.0		+1.0	μA
Output Leakage Current (note1)	I _{LO}		-1.0		+1.0	μA
V _{DD} Standby Current (note 1)	I _{CCS}	V _{DD} = V _{DD} Max. #CE = #RESET = V _{DD} ±0.2V, #WP = V _{DD} or V _{SS}		4	20	μA
V _{DD} Automatic Power Saving Current (note 1, 4)	I _{CCAS}	V _{DD} = V _{DD} Max. #CE = V _{SS} ±0.2V, #WP = V _{DD} or V _{SS}		4	20	μA
V _{DD} Reset Power-Down Current (note 1)	I _{CCD}	#RESET = V _{SS} ±0.2V		4	20	μA
Average V _{DD} Read Current Normal Mode (note1, 7)	I _{CCR}	V _{DD} = V _{DD} Max., #CE = V _{IL} , #OE = V _{IH} , f = 5 MHz		15	25	mA
Average V _{DD} Read Current Page Mode (note1, 7)			8 Word Read		5	10
V _{DD} (Page Buffer) Program Current (note 1, 5, 7)	I _{CCW}	V _{PP} = V _{PPH1}		20	60	mA
		V _{PP} = V _{PPH2}		10	20	mA
V _{DD} Block Erase, Full Chip Erase Current (note 1, 5, 7)	I _{CCE}	V _{PP} = V _{PPH1}		10	30	mA
		V _{PP} = V _{PPH2}		4	10	mA
V _{DD} (Page Buffer) Program or Block Erase Suspend Current (note 1, 2, 7)	I _{CCWS} I _{CCES}	#CE = V _{IH}		10	200	μA
V _{PP} Standby or Read Current (note 1, 6, 7)	I _{PPS} I _{PPR}	V _{PP} ≤ V _{DD}		2	5	μA
V _{PP} (Page Buffer) Program Current (note 1, 5, 6, 7)	I _{PPW}	V _{PP} = V _{PPH1}		2	5	μA
		V _{PP} = V _{PPH2}		10	30	mA
V _{PP} Block Erase, Full Chip Erase Current (note 1, 5, 6, 7)	I _{PPE}	V _{PP} = V _{PPH1}		2	5	μA
		V _{PP} = V _{PPH2}		5	15	mA
V _{PP} (Page Buffer) Program Suspend Current (note 1, 6, 7)	I _{PPWS}	V _{PP} = V _{PPH1}		2	5	μA
		V _{PP} = V _{PPH2}		10	200	μA
V _{PP} Block Erase Suspend Current (note 1, 6, 7)	I _{PPES}	V _{PP} = V _{PPH1}		2	5	μA
		V _{PP} = V _{PPH2}		10	200	μA

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DC Characteristics (continued)

PARAMETER	SYM.	TEST CONDITIONS	V _{DD} = 2.7V – 3.6V			UNIT
			Min.	Typ.	Max.	
Input Low Voltage (note 5)	V _{IL}		-0.4		0.4	V
Input High Voltage (note 5)	V _{IH}		V _{DD} -0.4		V _{DD} +0.4	V
Output Low Voltage (note 5)	V _{OL}	V _{DD} = V _{DD} Min., I _{OL} = 100 μA			0.2	V
Output High Voltage (note 5)	V _{OH}	V _{DD} = V _{DD} Min., I _{OH} = -100 μA	V _{DD} -0.2			V
V _{PP} Lockout during Normal Operations (note 3, 5, 6)	V _{PPLK}				0.4	V
V _{PP} during Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program Operations (note 6)	V _{PPH1}		1.65	3.0	3.6	V
V _{PP} during Block Erase, (Page Buffer) Program or OTP Program Operations (note 6)	V _{PPH2}		11.7	12	12.3	V
V _{DD} Lockout Voltage	V _{LKO}		1.5			V

Notes:

- All currents are in RMS unless otherwise noted. Typical values are the reference values at V_{DD} = 3.0V and T_A = +25° C unless V_{DD} is specified.
- I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or (page buffer) program is executed while in block erase suspend mode, the device's current draw is the sum of I_{CCES} and I_{CCR} or I_{CCW}. If read is executed while in (page buffer) program suspend mode, the device's current draw is the sum of I_{CCWS} and I_{CCR}.
- Block erases, full chip erase, (page buffer) program and OTP program are inhibited when V_{PP} ≤ V_{PPLK}, and not guaranteed in the range between V_{PPLK} (max.) and V_{PPH1} (min.), between V_{PPH1} (max.) and V_{PPH2} (min.) and above V_{PPH2} (max.).
- The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings (t_{AVQV}) provide new data when address are changed.
- Sampled, not 100% tested.
- V_{PP} is not used for power supply pin. With V_{PP} ≤ V_{PPLK}, block erase, full chip erase, (page buffer) program and OTP program cannot be executed and should not be attempted.
Applying 12V±0.3V to V_{PP} provides fast erasing or fast programming mode. In this mode, V_{PP} is power supply pin and supplies the memory cell current for block erasing and (page buffer) programming. Use similar power supply trace widths and layout considerations given to the V_{DD} power bus.
Applying 12V±0.3V to V_{PP} during erase/program can only be done for a maximum of 1,000 cycles on each block. V_{PP} may be connected to 12V±0.3V for a total of 80 hours maximum.
- The operating current in dual work is the sum of the operating current (read, erase, program) in each plane.

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AC Characteristics - Read-only Operations(1)

$V_{DD} = 2.7V$ to $3.6V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$

PARAMETER	SYM.	MIN.	MAX.	UNIT
Read Cycle Time	t_{AVAV}	70		nS
Address to Output Delay	t_{AVQV}		70	nS
#CE to Output Delay (note 3)	t_{ELQV}		70	nS
Page Address Access Time	T_{APA}		25	nS
#OE to Output Delay (note 3)	t_{GLQV}		20	nS
#RESET High to Output Delay	T_{PHQV}		150	nS
#CE or #OE to Output in High Z, whichever Occurs First (note 2)	t_{EHQZ}, t_{GHQZ}		20	nS
#CE to Output in Low Z (note 2)	T_{ELQX}	0		nS
#OE to Output in Low Z (note 2)	t_{GLQX}	0		nS
Output Hold from first Occurring Address, #CE or #OE Change (note 2)	t_{OH}	0		nS
Address Setup to #CE, #OE Going Low for Reading Status Register (note 4, 6)	t_{AVEL}, t_{AVGL}	10		nS
Address Hold from #CE, #OE Going Low for Reading Status Register (note 5, 6)	t_{ELAX}, t_{GLAX}	30		nS
#CE, #OE Pulse Width High for Reading Status Register (note 6)	t_{EHEL}, t_{GHGL}	20		nS

Notes:

1. See AC Input/Output Reference Waveform for timing measurements and maximum allowable input slew rate.
2. Sampled, not 100% tested.
3. #OE may be delayed up to t_{ELQV} to t_{GLQV} after the falling edge of #CE without impact to t_{ELQV} .
4. Address setup time (t_{AVEL}, t_{AVGL}) is defined from the falling edge of #CE or #OE (whichever goes low last).
5. Address hold time (t_{ELAX}, t_{GLAX}) is defined from the falling edge of #CE or #OE (whichever goes low last).
6. Specification s $t_{AVEL}, t_{AVGL}, t_{ELAX}, t_{GLAX}$, and t_{EHEL}, t_{GHGL} for read operations apply to only status register read operations.

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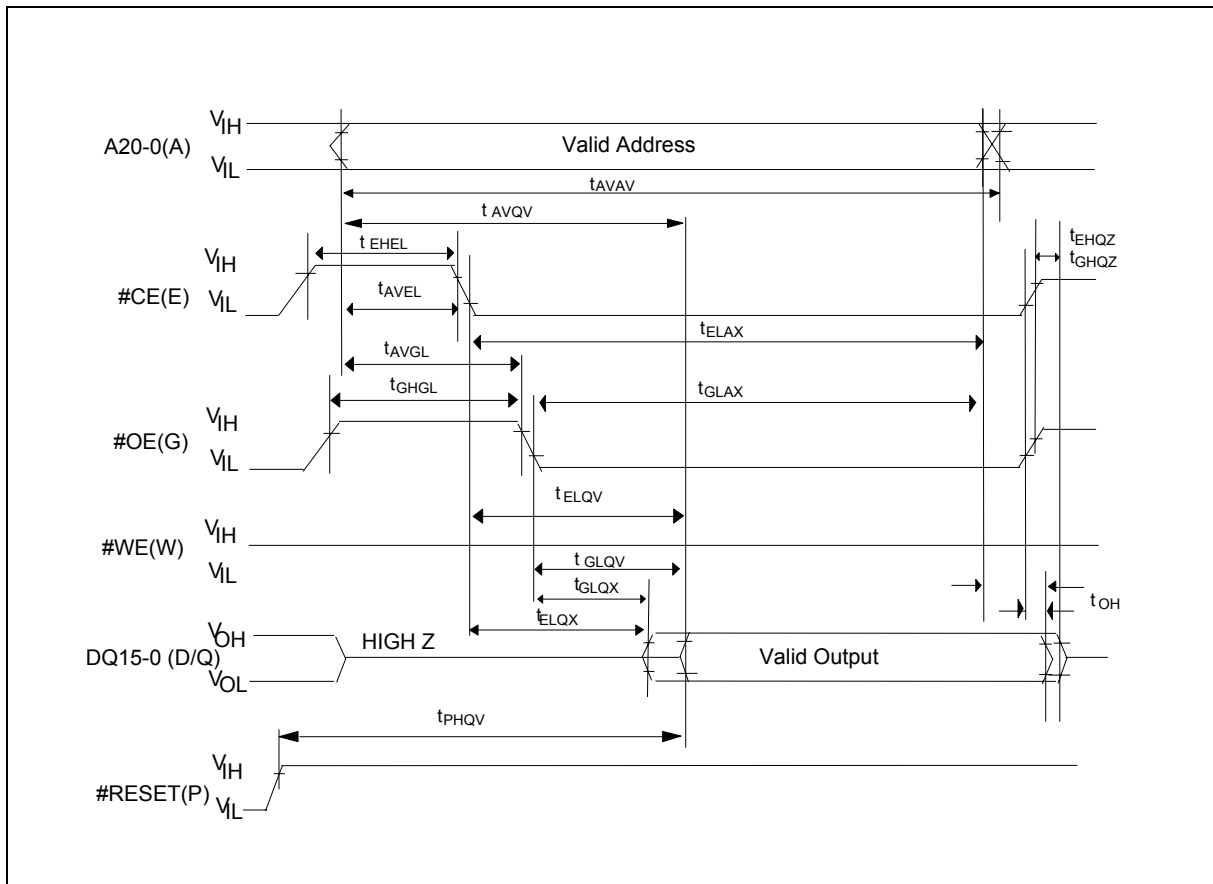


Figure 7. AC Waveform for Single Asynchronous Read Operations from Status Register, Identifier codes, OTP Block or Query Code

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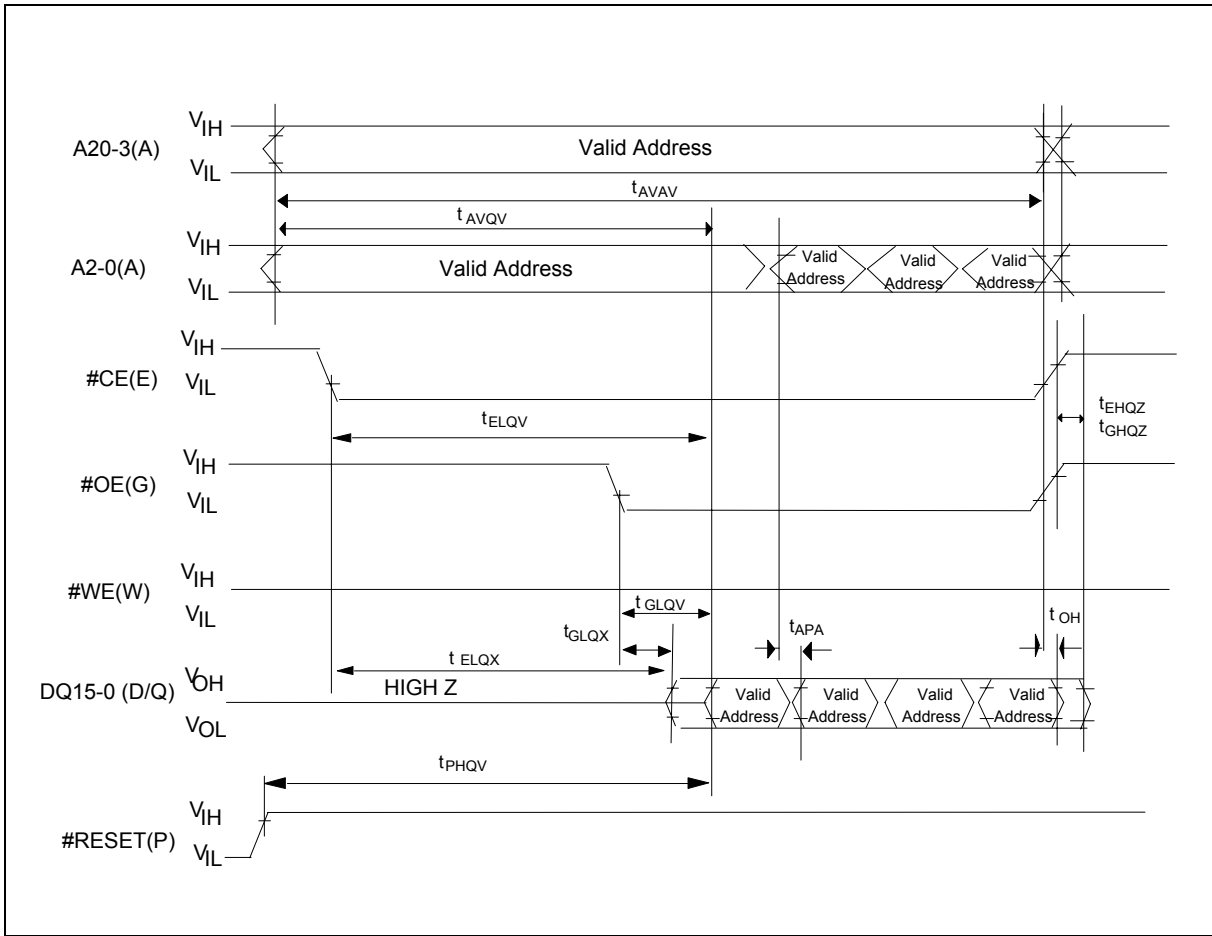


Figure 8. AC Waveform for Asynchronous 4-Word Page Mode Read Operations from Main Blocks or Parameter Blocks

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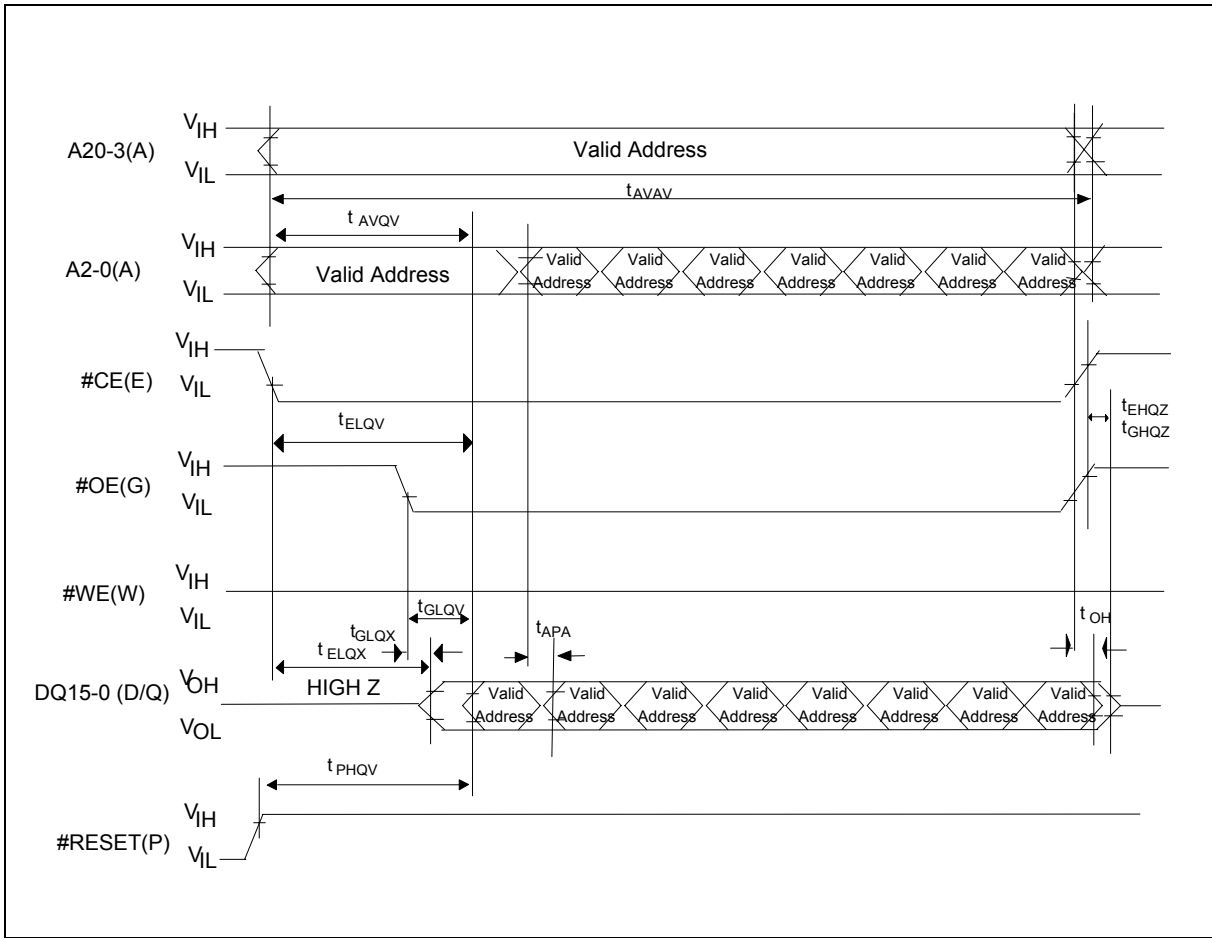


Figure 9. AC Waveform for Asynchronous 8-Word Page Mode Read Operations from Main Blocks or Parameter Blocks

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AC Characteristics - Write Operations^(1,2)

V_{DD} = 2.7V to 3.6V, T_A = -40°C to +85°C

PARAMETER	SYM.	MIN.	MAX.	UNIT
Write Cycle Time	t _{AVAV}	75		nS
#RESET High Recovery to #WE(#CE) Going Low (note 3)	t _{PHWL} (t _{PHL})	150		nS
#CE(#WE) Setup to #WE(#CE) Going Low	t _{ELWL} (t _{WLEL})	0		nS
#WE(#CE) Pulse Width (note 4)	t _{AVAV} = 75 nS t _{WLWH} (t _{LELH})	50		nS
Data Setup to #WE(#CE) Going High (note 8)	t _{DVWH} (t _{DVEH})	40		nS
Address Setup to #WE(#CE) Going High (note 8)	t _{AVWH} (t _{AVEH})	50		nS
#CE(#WE) Hold from #WE(#CE) High	t _{WHEH} (t _{EHWH})	0		nS
Data Hold from #WE(#CE) High	t _{WHDH} (t _{EHDH})	0		nS
Address Hold from #WE(#CE) High	t _{WHAX} (t _{EHAX})	0		nS
#WE(#CE) Pulse Width High (note 5)	t _{WHWL} (t _{EHEL})	25		nS
#WP High Setup to #WE(#CE) Going High (note 3)	t _{SHWH} (t _{SHEH})	0		nS
V _{PP} Setup to #WE(#CE) Going High (note 3)	t _{VVWH} (t _{VVEH})	200		nS
Write Recovery before Read	t _{WHGL} (t _{EHGL})	30		nS
#WP High Hold from Valid SRD (note 3, 6)	t _{QVSL}	0		nS
V _{PP} Hold from Valid SRD (note 3, 6)	t _{QVVL}	0		nS
#WE(#CE) High to SR.7 Going "0" (note 3, 7)	t _{WHR0} (t _{EHR0})		t _{AVQV} +40	nS

Notes:

- The timing characteristics for reading the status register during block erase, full chip erase, (page buffer) program and OTP program operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
- A write operation can be initiated and terminated with either #CE or #WE.
- Sampled, not 100% tested.
- Write pulse width (t_{WP}) is defined from the falling edge of #CE or #WE (whichever goes low last) to the rising edge of #CE or #WE (whichever goes high first). Hence, t_{WP} = t_{WLWH} = t_{LELH} = t_{WLEH} = t_{ELWH}.
- Write pulse width high (t_{WPH}) is defined from the rising edge of #CE or #WE (whichever goes high first) to the falling edge of #CE or #WE (whichever goes low last). Hence, t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}.
- V_{PP} should be held at V_{PP} = V_{PPH1/2} until determination of block erase, full chip erase, (page buffer) program or OTP program success (SR.1/3/4/5 = 0).
- t_{WHR0} (t_{EHR0}) after the Read Query or Read Identifier Codes/OTP command = t_{AVQV}+100 nS.
- Refer to Table 6 for valid address and data for block erase, full chip erase, (page buffer) program, OTP program or lock bit configuration.

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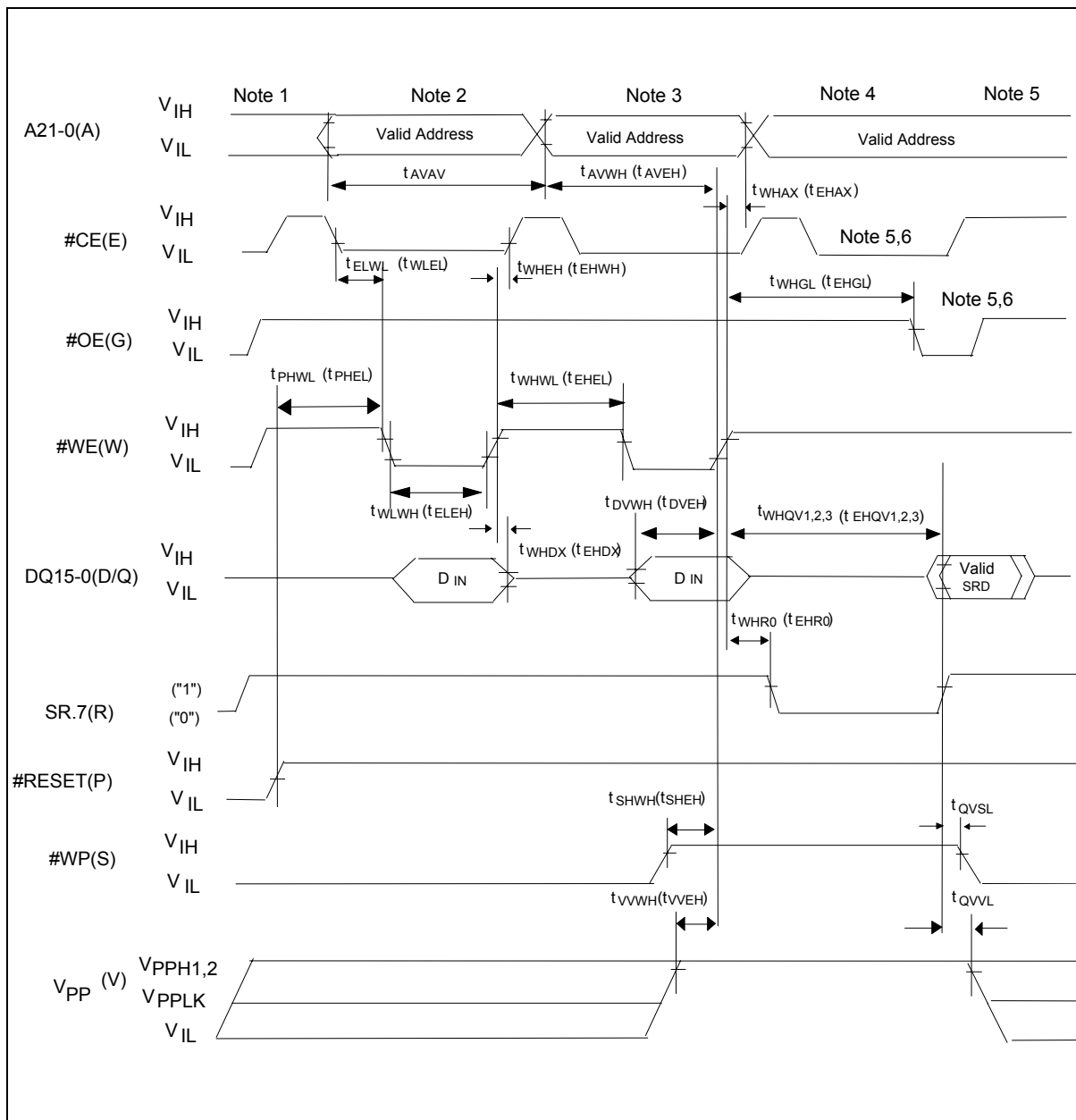


Figure 10. AC Waveform for Write Operations

Notes:

1. V_{DD} power-up and standby.
2. Write each first cycle command.
3. Write each second cycle command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. For read operation, #OE and #CE must be driven active, and #WE de-asserted.



Reset Operations

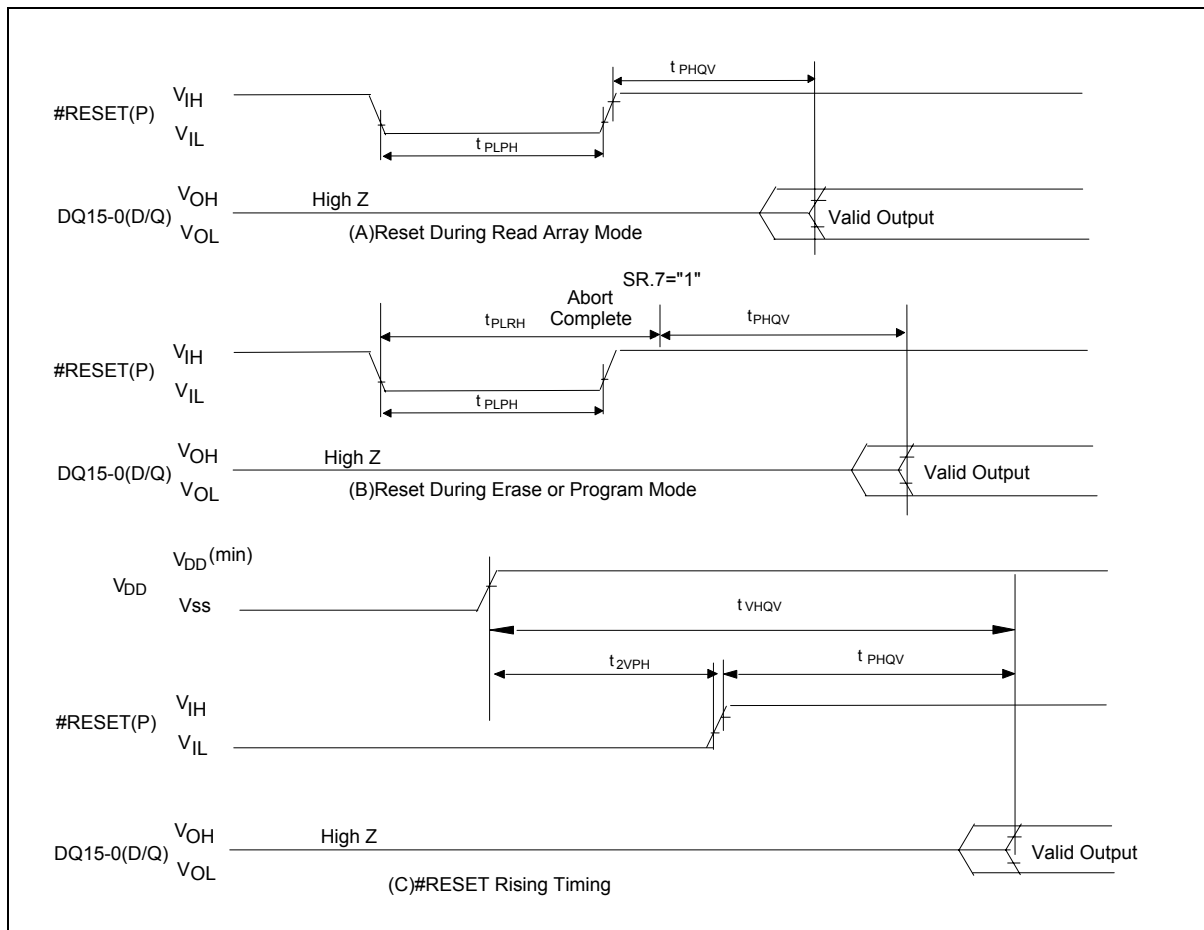


Figure 11. AC Waveform for Reset Operation

Reset AC Specifications

$V_{DD} = 2.7V$ to $3.6V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$

PARAMETER	SYM.	MIN.	MAX.	UNIT
#RESET Low to Reset during Read (#RESET should be low during power-up.) (note 1, 2, 3)	t_{PLPH}	100		nS
#RESET Low to Reset during Erase or Program (note 1, 3, 4)	t_{PLRH}		22	μS
V_{DD} 2.7V to #RESET High (note 1, 3, 5)	t_{2VPH}	100		nS
V_{DD} 2.7V to Output Delay (note 3)	t_{VHQV}		1	mS

Notes:

1. A reset time, t_{PHQV} , is required from the later of SR.7 going "1"(High Z) or #RESET going high until outputs are valid. Refer to AC Characteristics - Read-Only Operations for t_{PHQV} .
2. t_{PLPH} is <100ns the device may still reset but this is not guaranteed.
3. Sampled, not 100% tested.

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- If #RESET asserted while a block erase, full chip erase, (page buffer) program or OTP program operation is not executing, the reset will complete within 100ns.
- When the device power-up, holding #RESET low minimum 100ns is required after V_{DD} has been in predefined range and also has been in stable there.

Block Erase, Full Chip Erase, (Page Buffer) Program and OTP Program Performance⁽³⁾

V_{DD} = 2.7V to 3.6V, T_A = -40°C to +85°C

PARAMETER	SYM.	PAGE BUFFER COMMAND IS USED OR NOT USED	V _{PP} = V _{PPH1} (IN SYSTEM)			V _{PP} = V _{PPH2} (IN MANUFACTURING)			UNIT
			MIN.	TYP. ⁽¹⁾	MAX. ⁽²⁾	MIN.	TYP. ⁽¹⁾	MAX. ⁽²⁾	
4K-Word Parameter Block Program Time (note 2)	t _{WPB}	Not Used		0.05	0.3		0.04	0.12	S
		Used		0.03	0.12		0.02	0.06	S
32K-Word Main Block Program Time (note 2)	t _{WMB}	Not Used		0.38	2.4		0.31	1.0	S
		Used		0.24	1.0		0.17	0.5	S
Word Program Time (note 2)	t _{WHQV1/} t _{EHQV1}	Not Used		11	200		9	185	μS
		Used		7	100		5	90	μS
OTP Program Time (note 2)	t _{WHOV1/} t _{EHOV1}	Not Used		36	400		27	185	μS
4K-Word Parameter Block Erase Time (note 2)	t _{WHQV2/} t _{EHQV2}	-		0.3	4		0.2	4	S
32K-Word Main Block Erase Time (note 2)	t _{WHQV3/} t _{EHQV3}	-		0.6	5		0.5	5	S
Full Chip Erase Time (note 2)				40	350		33	350	S
(Page Buffer) Program Suspend Latency Time to Read (note 4)	t _{WHRH1/} t _{EHRH1}	-		5	10		5	10	μS
Block Erase Suspend Latency Time to Read (note 4)	t _{WHRH2/} t _{EHRH2}	-		5	20		5	20	μS
Latency Time from Block Erase Resume Command to Block Erase Suspend Command (note 5)	t _{ERES}	-	500			500			μS

Notes:

- Typical values measured at V_{DD} = 3.0V, V_{PP} = 3.0V or 12V, and T_A = +25°C. Assumes corresponding lock bits are not set. Subject to change based on device characterization.
- Excludes external system-level overhead.
- Sampled, but not 100% tested.
- A latency time is required from writing suspend command (#WE or #CE going high) until SR.7 going "1".
- If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than t_{ERES} and its sequence is repeated, the block erase operation may not be finished.

5. ADDITIONAL INFORMATION

Recommended Operating Conditions

At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

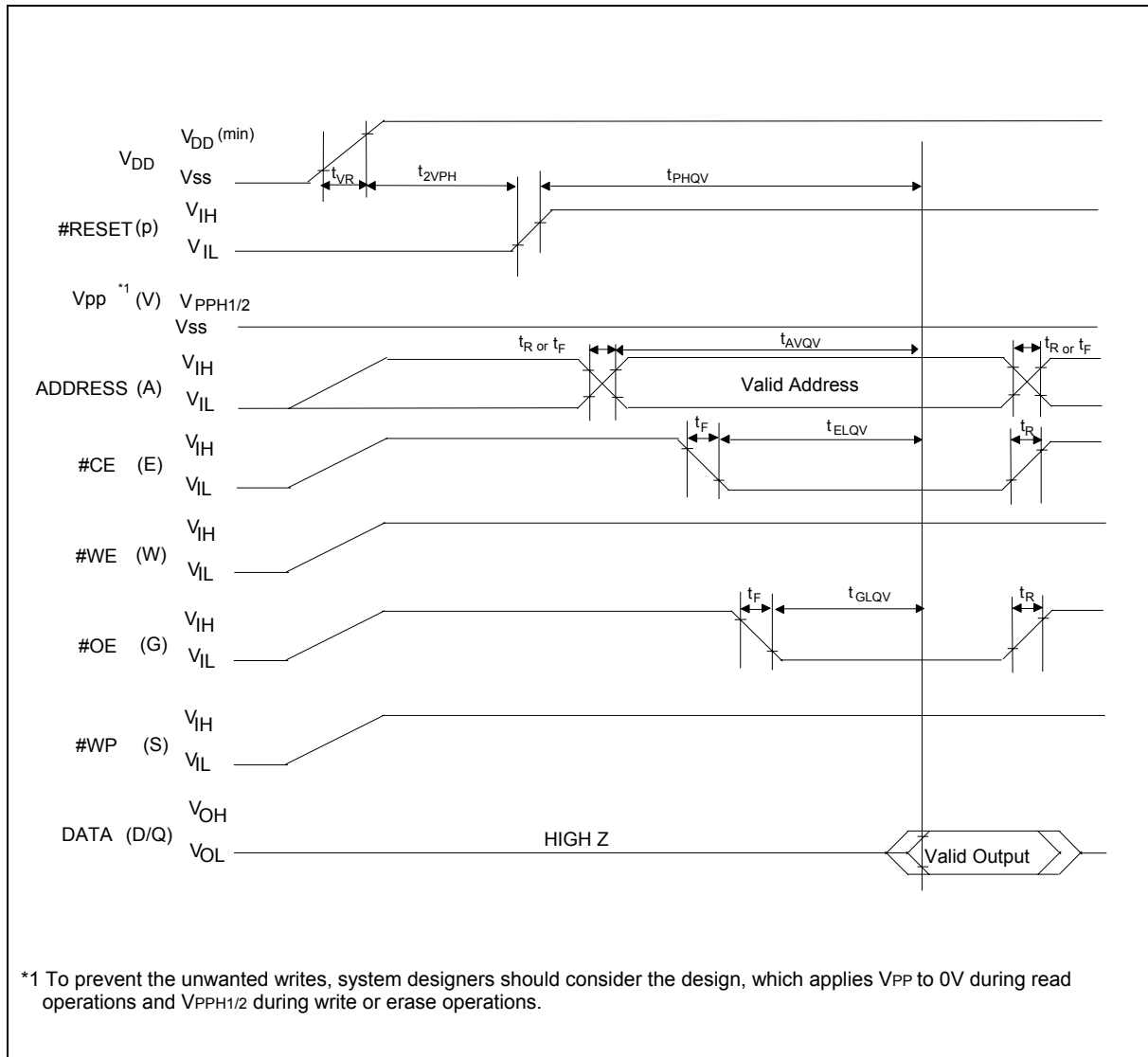


Figure A-1. AC Timing at Device Power-up

For the AC specifications t_{VR} , t_R , t_F in the figure, refer to the next page. See the "ELECTRICAL SPECIFICATIONS" described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

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Rise and Fall Time

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
V_{DD} Rise Time (note 1)	t_{VR}	0.5	30000	$\mu\text{S}/\text{V}$
Input Signal Rise Time (note1, 2)	t_R		1	$\mu\text{S}/\text{V}$
Input Signal Fall Time (note1, 2)	t_F		1	$\mu\text{S}/\text{V}$

Notes:

1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.

Glitch Noises

Do not input the glitch noises which are below V_{IH} (Min.) or above V_{IL} (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).

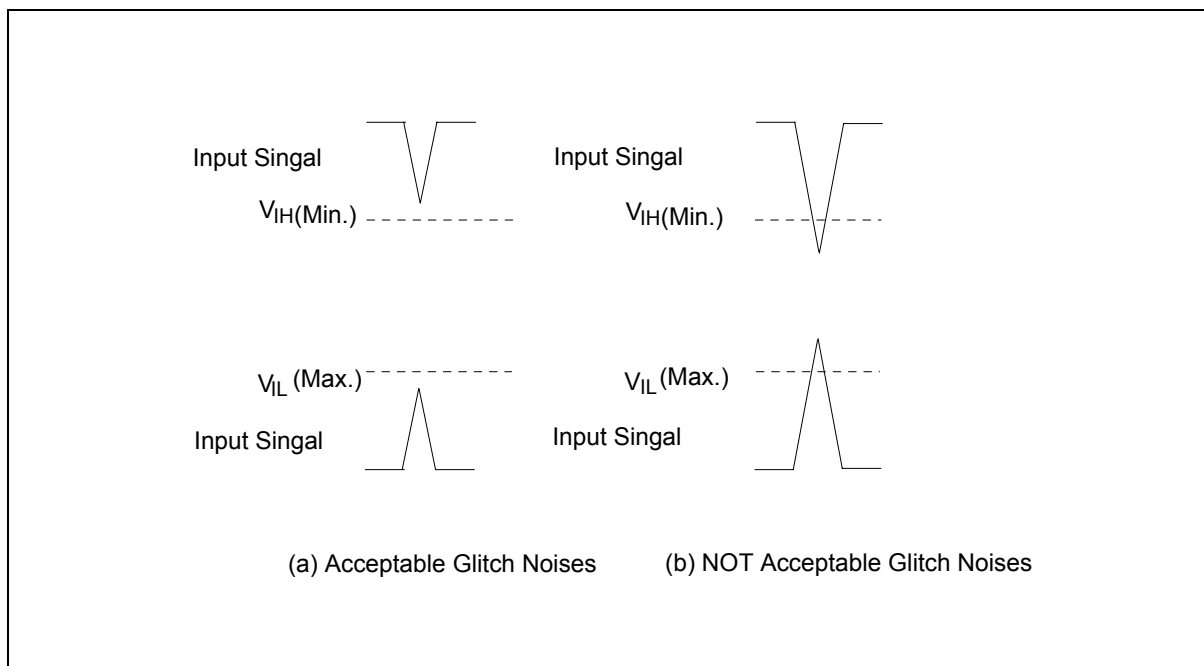


Figure A-2. Waveform for Glitch Noises

See the "DC CHARACTERISTICS" described in specifications for V_{IH} (Min.) and V_{IL} (Max.).

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6. ORDERING INFORMATION

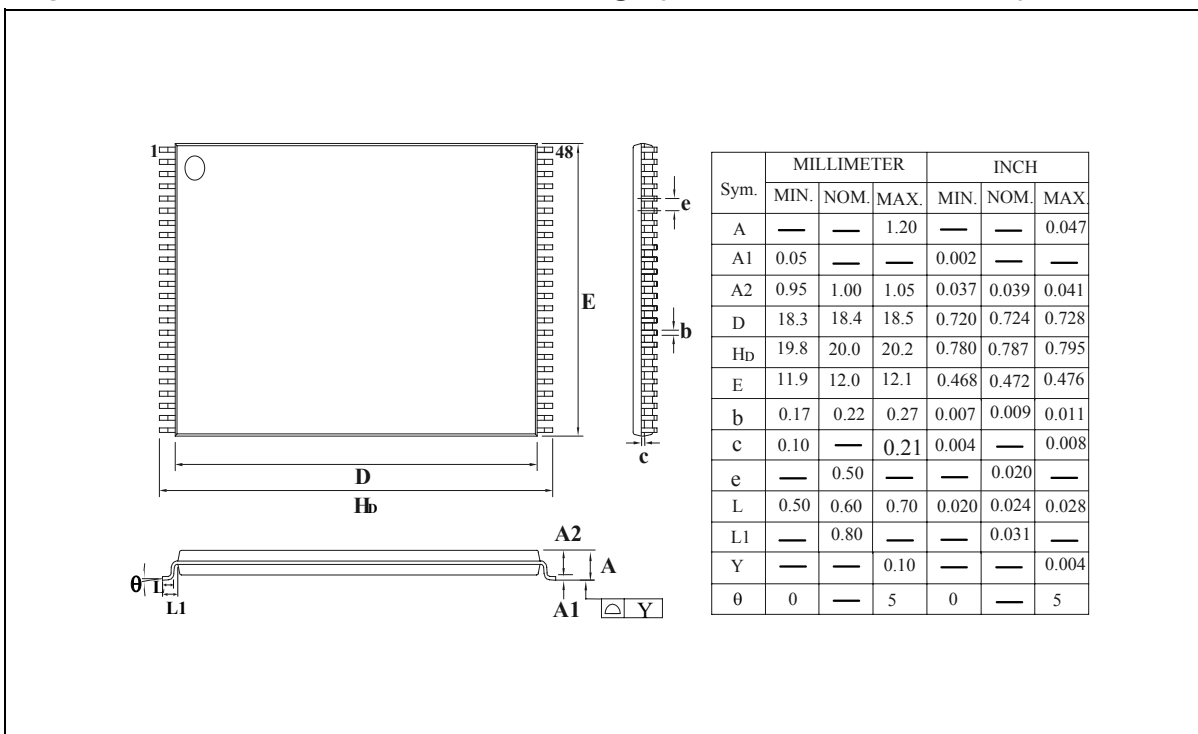
PART NO.	ACCESS TIME (nS)	OPERATING TEMPERATURE (°C)	BOOT BLOCK	PACKAGE
W28F321BT70L	70	-40° C to 85° C	Bottom Boot	48-Pin TSOP
W28F321TT70L	70	-40° C to 85° C	Top Boot	48-Pin TSOP

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

7. PACKAGE DIMENSION

48-pin Standard Thin Small Outline Package (measured in millimeters)



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8. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Jan. 6, 2003	-	Initial Issued



Headquarters

No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
<http://www.winbond.com.tw/>

Taipei Office

9F, No.480, Rueiguang Rd.,
Neihu District, Taipei, 114,
Taiwan, R.O.C.
TEL: 886-2-8177-7168
FAX: 886-2-8751-3579

Winbond Electronics Corporation America

2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441798

Winbond Electronics Corporation Japan

7F Daini-ueno BLDG, 3-7-18
Shinyokohama Kohoku-ku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Winbond Electronics (Shanghai) Ltd.

27F, 2299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62365998

Winbond Electronics (H.K.) Ltd.

Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

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